Please enter the following amendments:

In the Specification:

On pages 9 and 10, amend paragraph [0027] as follows:

[0027] The magnetic moment vectors in the two ferromagnetic layers 30, 32 and 60, 62 in each of the bits 18 and 20 of the MRAM device 12 may have different thicknesses or material to provide a resultant magnetic moment vector given by ~~nMnn~~ ΔM_{86} =(M_{84}-M_{82}) ~~Mnn, M92, M84~~ and a sub-layer moment fractional balance ratio, $M_{br} = \frac{(M_{84} - M_{82})}{(M_{84} + M_{82})} = \frac{\Delta M_{86}}{M_{total}}$. The vectors in these equations are identified for simplification for bit 18 only. The equations would apply equally to bit 20. The resultant magnetic moment vector of the multilayer structures 22 and multilayer structure 52 is free to rotate with an applied magnetic field. In zero field the resultant magnetic moment vectors 86 and 94 will be stable in a direction, determined by the magnetic anisotropy, that is either parallel or anti-parallel with respect to the resultant magnetic moment vector of the pinned reference layer 42 or 72, respectively. It will be understood that the term "resultant magnetic moment vector" is used only for purposes of this description and for the case of totally balanced moments, the resultant magnetic moment vector can be zero in the absence of a magnetic field. As described below, only the sub-layer magnetic moment vectors 84 and 92 adjacent to the tunnel barrier determine the state of the bits 18 and 20, respectively.

On page 13, amend paragraph [0034] as follows:

[0034] As previously mentioned, bit 20 functions similarly to bit 18; however in this first embodiment as described, the tunnel barriers 24 and 54 are deposited with different thicknesses, giving a different resistance range for each bit 18 and 20, such as 2K and 4K ohms with MR of 50%. For example, MR = ~~a~~R $\Delta R/R_{low} = (R_{high} - R_{low})/R_{low}$. For 2 bits, 4 separate resistance states may be determined as shown in the chart below.

	BIT 2 (0)	BIT 2 (1)
BIT 1 (0)	$R^1_{low} + R^2_{low}$	$R^1_{high} + R^2_{low}$
BIT 1 (1)	$R^1_{low} + R^2_{high}$	$R^1_{high} + R^2_{high}$

On page 20, amend paragraph [0050] as follows:

[0050] There are seven regions of operation illustrated in FIG. 7 for the second embodiment which includes both a direct and a toggle mode. In a region 114 there is no switching, e.g., there is not sufficient current in either the word line 14 or digit line 16 to create a strong enough magnetic field to "write" the bits 18 and 20. For MRAM operation in ~~a~~ regions [~~118~~] 118, 130 and 134, the direct writing method is in effect for writing bit 18 (region 130) and bit 20 (region 134)[,]. When using the direct writing method, there is no need to determine the initial state of the MRAM device because the state is only switched if the state being written is different from the state that is stored. The selection of the written state is determined by the direction of current in both word line 14 and digit line 16. For example, if a '1' is desired to be written, then the direction of current in all the lines will be positive. If a '1' is already stored in the element and a '1' is being

written, then the final state of the MRAM device will continue to be a '1'. Further, if a '0' is stored and a '1' is being written with positive currents, then the final state of the MRAM device will be a '1'. Similar results are obtained when writing a '0' by using negative currents in both the word and digit lines. Hence, either state can be programmed to the desired '1' or '0' with the appropriate polarity of current pulses, regardless of its initial state.